What is claimed is:

1. A real time control system of a multitasking digital signal processor, comprising:

a ready queue including a ready queue link having first information indicating the task control block for the first task among tasks in the digital signal processor, and the task control block for the last task, and a priority link group of priority links, the number of which is the same as the number of priority levels, having second information indicating the task control block for the first task among tasks of the same priority among the tasks, and the task control block for the last task; and

an operating system for setting the first and second information according to the conditions of tasks for the digital signal processor, and controlling switching between the tasks of the ready queue.

2. The real time control system of claim 1, wherein each of the first and second information includes a list pointer corresponding to the task control block of the first task and a last pointer corresponding to the task control block of the last task.

3. The real time control system of claim 1, wherein the operating system updates the first and second information so that deterministic scheduling with respect to the ready queue link and the priority link is maintained, when a task for the digital signal processor is inserted or deleted.

4. The real time control system of claim 1, further comprising a waiting queue including a waiting queue link including third information indicating the task control block for the first task among tasks in the digital signal processor, and the task control block for the last task, and a priority link group of priority links, the number of which is the same as the number of priority levels, having fourth information indicating the task control block for the first task among tasks of the same priority among the tasks, and the task control block for the last task, wherein the operating system sets the third and fourth information so that resources for the tasks of the waiting queue are deterministically acquired.

5. The real time control system of claim 4, wherein each of the third and fourth information includes a list pointer corresponding to the task control block of the first task and a last pointer corresponding to the task control block of the last task.

6. The real time control system of claim 1, wherein the operating system controls the ready queue so that switching between tasks is achieved on the basis of the priority link group, when task searching in the digital signal processor is based on the priority order, and controls the ready queue so that switching between tasks is achieved on the basis of the ready queue link, when the task searching is based on a first-in first-out (FIFO) system.

7. The real time control system of claim 1, further comprising a timer wheel for managing the timer control blocks for the tasks in a pointer arrangement structure, wherein the operating system inserts the timer control blocks into corresponding slots of the timer wheel according to the time set for the tasks.

8. The real time control system of claim 7, wherein the timer wheel is divided into two timer wheels according to a predetermined reference time, and the operating system inserts timer control blocks corresponding to the slots of the first timer wheel when the time set for the tasks are equal to or less than the reference time, and inserts timer control blocks corresponding to the slots of the second timer wheel when the time set for the tasks are greater than the reference time and equal to or less than twice the reference time.

9. The real time control system of claim 8, wherein the operating system generates errors when the time set for the tasks are greater than twice the reference time.

10. The real time control system of claim 1, wherein a memory used to process the tasks in the digital signal processor is divided into an internal memory

and an external memory in the digital signal processor, and the operating system manages the internal memory and the external memory using a memory structure made up of a start address, an end address, a memory size, a memory map, and next information indicating the start address of the next memory to be connected.

11. The real time control system of claim 10, wherein the operating system manages the memory so that the internal memory is allocated when the digital signal processor is required to perform fast processing on a task, and so that the external memory is allocated when the internal memory is completely allocated.

12. The real time control system of claim 10, wherein the operating system manages the memory so that the external memory is divided into a plurality of memories using the memory structure.

13. The real time control system of claim 10, wherein the operating system allocates and returns the memory in units of predetermined-sized pages in a system call way, and checks allocation or non-allocation of the memory on the basis of the map of the memory.